AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-6. (Cancelled)

7. (new) A serial communication device, comprising:

a central processing unit for executing a program;

a serial communication interface coupled to receive data from an outside of the serial communication device and providing a transfer request signal and a timeout interrupt signal, wherein the timeout interrupt signal is provided to the central processing unit when the data from the outside of the serial communication device is stopped for a certain time;

a RAM including:

a buffer area for storing the data, and

a work area for the program; and

a direct memory access controller coupled to receive the transfer request signal and transferring the data from the serial communication interface to the buffer area, the direct memory access controller being set therein a first number as a number of transfer which is larger than a second

number of data received at a time by the serial communication interface,

wherein the direct memory access controller provides a data transfer end interrupt signal to the central processing unit when a transfer number of data received by the serial communication interface reaches the first number, and

wherein the data stored in the buffer area is transferred to the work area by the direct memory access controller when the central processing unit receive the data transfer end interrupt signal or the timeout interrupt signal.

8. (new) A serial communication device according to claim 7,

wherein the serial communication interface includes a first-in first-out memory in which the data from the outside of the serial communication device is stored, and

wherein the transfer request signal is provided to the direct memory access controller when a number of data received in the first-in first-out memory is exceeded a number of received trigger set in the serial communication interface.

9. (new) A serial communication device according to claim 7,

wherein the direct memory access controller is started up before the serial communication interface receives the data, and

wherein the first number is set in the direct memory access controller before the serial communication interface receives the data.

10. (new) A serial communication device according to claim 9, wherein the serial communication interface further includes: a means stopping the generation of the next data receive after the timeout interrupt signal has been once generated.

11. (new) A serial communication device comprising:

a central processing unit for executing a program;

a serial communication interface coupled to receive data from an outside of the serial communication device and providing a transfer request signal, the serial communication interface including a timeout interrupt signal generation section for providing a timeout interrupt signal to the central processing unit according to a timeout

setting value for a period until the timeout interrupt signal is generated;

a memory including:

a buffer area for storing the data, and

a work area for the program; and

a direct memory access controller coupled to receive the transfer request signal and transferring the data from the serial communication interface to the buffer area, the direct memory access controller being set therein a first number as a number of transfers which is larger than a second number as a number of data received at a time by the serial communication interface,

wherein the direct memory access controller provides a data transfer end interrupt signal to the central processing unit when a number of data transferred from the serial communication interface to the buffer area by the direct memory access controller reaches the first number, and

wherein the data stored in the buffer area is transferred to the work area by the direct memory access controller when the central processing unit receive one of the data transfer end interrupt signal and the timeout interrupt signal.

12. (new) A serial communication device according to claim 11, wherein the timeout interrupt signal generation section includes:

a receive determination section coupled to receive the data from outside of the serial communication device and providing a count start trigger when the data is received;

a counter coupled to receive the count start trigger and providing a count value; and

an overflow determination section coupled to receive the count value and the timeout setting value and providing the timeout interrupt signal when the count value is exceeded the timeout setting value.

13. (new) A serial communication device according to claim 12, wherein the timeout interrupt signal generation section further includes a register for storing the timeout setting value.

14. (new) A serial communication device according to claim 13, wherein the serial communication interface further has function for stopping the generation of the timeout interrupt signal until the next data receive by the serial communication interface after the timeout interrupt signal has been once provided.

15. (new) A serial communication device according to claim 11,

wherein the serial communication interface includes a first-in first-out memory in which the data from the outside of the serial communication device is stored, and

wherein the transfer request signal is provided to the direct memory access controller when a number of data received in the first-in first-out memory exceeded a number of received trigger set in the serial communication interface.

16. (new) A serial communication device according to claim 11,

wherein the direct memory access controller is started up before the serial communication interface receives the data, and

wherein the first number is set in the direct memory access controller before the serial communication interface receives the data.

17. (new) A serial communication device comprising:

a central processing unit for executing a program;

a serial communication interface coupled to receive data from an outside of the serial communication device and providing a transfer request signal, the serial communication interface including a timeout interrupt signal generation section for providing a timeout interrupt signal to the central processing unit according to a timeout value for a time period until the timeout interrupt signal is generated;

a memory including:

a first buffer area,

a second buffer area, and

a work area for the program; and

a direct memory access controller having a continuous transfer function and coupled to receive the transfer request signal and transferring the data from the serial communication interface to one of the first buffer area and the second buffer area, the direct memory access controller providing a data transfer end interrupt signal to the central processing unit and changing a destination of a data transfer to the other of the first buffer area and the second buffer area is full with the data,

wherein the data stored in the one of the first buffer area and the second buffer area is transferred to the work area by the direct memory access controller when the central

processing unit receive one of the data transfer end interrupt signal and the timeout interrupt signal.

18. (new) A serial communication device according to claim 17,

wherein the serial communication interface includes a first-in first-out memory where the data from the outside of the serial communication device is stored, and

wherein the transfer request signal is provided to the direct memory access controller when a number of data received in the first-in first-out memory exceeded a number of received trigger set in the serial communication interface.

19. (new) A serial communication device according to claim 17,

wherein the direct memory access controller is started up before the serial communication interface receives the data, and

wherein the first number is set in the direct memory access controller before the serial communication interface receives the data.

20. (new) A serial communication device according to claim 17,

wherein the timeout interrupt signal generation section includes:

a receive determination section coupled to receive the data from the outside of the serial communication device and providing a count start trigger when determining a reception of the data by the serial communication interface;

a counter responsive to the count start trigger and starting its count up operation and providing a count value; and

an overflow determination section comparing the count value with the timeout setting value and providing the timeout interrupt signal according to a result of the comparison that the count value is exceeded the timeout setting value.

21. (new) A serial communication device according to claim 20, wherein the timeout interrupt signal generation section further includes a register for storing the timeout setting value.

22. (new) A serial communication device according to claim 20,

wherein the direct memory access controller has a first channel and a second channel,

wherein one of the first channel and the second channel is used for a data transfer from the serial communication unit to the one of the first buffer area and the second buffer area while the other of the first channel and the second channel is used for a data transfer from the other of the first buffer area and the second buffer area to the work area.

23. (new) A serial communication device according to claim 17, wherein the serial communication interface further includes a function to stop the generation of the timeout interrupt signal until the serial communication interface receives next data after the timeout interrupt signal is provided.